

# ESP32 Datasheet



**Espressif Systems**

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## About This Guide

This document provides introduction to the specifications of ESP32 hardware.

The document structure is as follows:

| Chapter   | Title                     | Subject  |
|-----------|---------------------------|--|
| Chapter 1 | Overview                  | An overview of ESP32, including featured solutions, basic and advanced features, applications and development support. |
| Chapter 2 | Pin Definitions           | Introduction to the pin layout and descriptions.   |
| Chapter 3 | Functional Description    | Description of the major functional modules.   |
| Chapter 4 | Peripheral Interface      | Description of the peripheral interfaces integrated on ESP32.  |
| Chapter 5 | Electrical Specifications | The electrical characteristics and data of ESP32.  |
| Chapter 6 | Package Information       | The package details of ESP32.  |
| Chapter 7 | Supported Resources       | The related documents and community resources for ESP32.   |
| Chapter 8 | Appendix - Touch Sensor   | The touch sensor design and layout guidelines.   |

## Release Notes

| Date    | Version | Release notes  |
|---------|---------|----------------|
| 2016.05 | V1.0    | First release. |

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# 1. Overview

ESP32 is a single chip 2.4 GHz Wi-Fi and Bluetooth combo chip designed with TSMC ultra low power 40 nm technology. It is designed and optimized for the best power performance, RF performance, robustness, versatility, features and reliability, for a wide variety of applications, and different power profiles.

## 1.1 Featured Solutions

### 1.1.1 Ultra Low Power Solution

ESP32 is designed for mobile, wearable electronics, and Internet of Things (IoT) applications. It has many features of the state-of-the-art low power chips, including fine resolution clock gating, power modes, and dynamic power scaling. For instance, in a low-power IoT sensor hub application scenario, ESP32 is woken up periodically and only when a specified condition is detected; low duty cycle is used to minimize the amount of energy that the chip expends. The output power of the power amplifier is also adjustable to achieve an optimal trade off between communication range, data rate and power consumption.

**Note:**

For more information, please refer to Section 3.10 Low-Power Management.

### 1.1.2 Complete Integration Solution

ESP32 is the most integrated solution for Wi-Fi + Bluetooth applications in the industry with less than 10 external components. ESP32 integrates the antenna switches, RF balun, power amplifier, low noise receive amplifier, filters, and power management modules. As such, the entire solution occupies minimal Printed Circuit Board (PCB) area.

ESP32 also integrates advanced calibration circuitries that allow the solution to dynamically adjust itself to remove external circuit imperfections or adjust to changes in external conditions.

As such, the mass production of ESP32 solutions does not require expensive and specialized Wi-Fi test equipment.

## 1.2 Basic Protocols

### 1.2.1 Wi-Fi

- 802.11 b/g/n/e/i
  - 802.11 n (2.4 GHz), up to 150 Mbps
  - 802.11 i security features: pre-authentication and TSN
  - 802.11 e: multiple queue management to fully utilize QoS traffic prioritization
  - Wi-Fi Protected Access (WPA)/WPA2
  - Wi-Fi Protected Setup (WPS)
- A-MPDU and A-MSDU aggregation
- Fragmentation and defragmentation



- SSL stacks with hardware accelerators
- Automatic beacon monitoring/scanning
- Infrastructure BSS Station mode/ Soft AP mode
- Wi-Fi Direct (P2P), P2P Discovery, P2P Group Owner mode and P2P Power Management
- UMA compliant and certified
- Antenna diversity and selection
- WMM power save U-APSD

**Note:**

For more information, please refer to Section 3.9 Wi-Fi.

## 1.2.2 Bluetooth

- CMOS single-chip fully-integrated radio and baseband
- Bluetooth Piconet and Scatternet
- Compliant with Bluetooth v4.2 BR/EDR and BLE specification
- Adaptive Frequency Hopping (AFH)
- Security Manage Protocol (SMP)
- Class-1, class-2 and class-3 transmitter without external power amplifier
- +10 dBm transmitting power
- NZIF receiver with -90 dBm sensitivity
- High speed UART HCI, up to 4 Mbps
- SDIO / SPI HCI
- CVSD and SBC for audio codec
- Low power consumption

## 1.3 MCU and Advanced Features

### 1.3.1 CPU and Memory

- Xtensa® Dual-Core 32-bit LX6 microprocessors, up to 400 MIPS
- 128 kB ROM
- 512 kB SRAM
- QSPI Flash/SRAM, up to 4 x 16 MB
- Power supply: 2.5 V to 3.6 V

### 1.3.2 Clocks and Timers

- 2 MHz to 40 MHz crystal oscillator
- Internal 8 MHz oscillator with calibration
- External 32 kHz oscillator for RTC with calibration
- Internal RC oscillator with calibration
- Two timer groups including 3 x 64-bit timers and 1 x watchdog in each group
- RTC timer with sub-second accuracy
- RTC watchdog

### 1.3.3 Advanced Peripheral Interfaces

- 12-bit SAR ADC up to 16 channels
- 2 x 10-bit D/A converters
- 10 x touch sensors
- Temperature sensor
- 4 x SPI
- 2 x I2S
- 2 x I2C
- 2 x UART
- 1 host (SD/eMMC/SDIO)
- 1 slave (SDIO/SPI)
- Ethernet MAC interface with dedicated DMA and IEEE 1588 support
- CAN 2.0
- IR (TX/RX)
- Motor PWM
- LED PWM up to 16 channels

### 1.3.4 Security

- IEEE 802.11 standard security features all supported, including WPA, WPA/WPA2 and WAPI
- Secure boot
- Flash encryption
- 1024-bit OTP, up to 768-bit for customers
- Cryptographic hardware acceleration:
  - AES 128/192/256
  - HASH (SHA-2) library

- RSA
- Radom Number Generator

### 1.3.5 Development Support

- SDK Firmware for fast on-line programming
- Open source toolchains based on GCC

**Note:**

For more information, please refer to Chapter 7 Supported Resources.

## 1.4 Applications

- Generic low power IOT sensor hub
- Generic low power IOT loggers
- Video streaming from camera
- Wi-Fi + Bluetooth enabled Over The Top (OTT) devices
- Wi-Fi + Bluetooth enabled smart devices
- Music players
  - Internet music players
  - Wi-Fi + Bluetooth audio streaming devices
- Wi-Fi enabled toys
  - Loggers
  - Proximity sensing toys
- Wi-Fi enabled speech recognition devices
- Audio headsets
- Smart power plugs
- Home automation
- Mesh network
- Industrial wireless control
- Baby monitors
- Sensor networks
- Wearable electronics
- Wi-Fi location-aware devices
- Security ID tags
- Healthcare

- Proximity and movement monitoring trigger devices
- Temperature sensing loggers

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## 2. Pin Definitions

### 2.1 Pin Layout

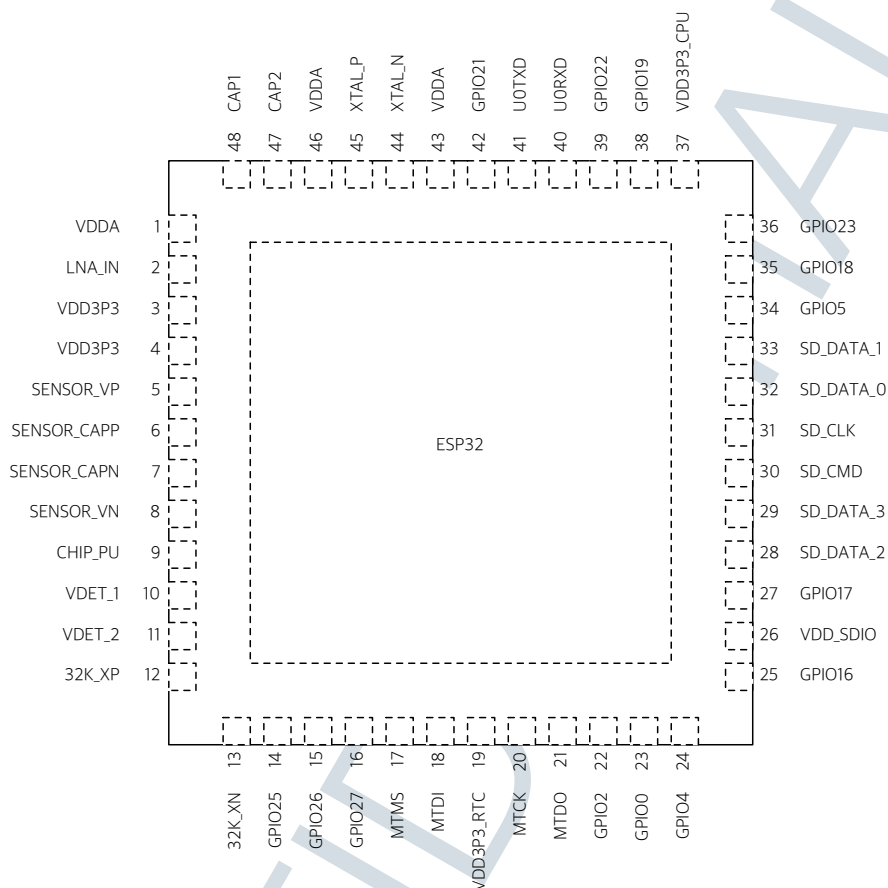


Figure 1: ESP32 Pin Layout

### 2.2 Pin Description

Table 1: Pin Description

| Name      | No. | Type | Function   |
|-----------|-----|------|--|
| VDDA      | 1   | P    | Analog power supply (2.3V - 3.6V)  |
| LNA_IN    | 2   | I/O  | RF input and output  |
| VDD3P3    | 3   | P    | Amplifier power supply (2.3V - 3.6V)   |
| VDD3P3    | 4   | P    | Amplifier power supply (2.3V - 3.6V)   |
| SENSOR_VP | 5   | I    | GPIO36, SENSOR_VP, ADC_PRE_AMP, ADC1_CH0, RTC_GPIO0<br>Note: Connects 270pF capacitor from SENSOR_VP to SENSOR_CAPP. |

| Name        | No. | Type | Function   |
|-------------|-----|------|--|
| SENSOR_CAPP | 6   | I    | GPIO37, SENSOR_CAPP, ADC_PRE_AMP, ADC1_CH1, RTC_GPIO1<br>Note: Connects 270pF capacitor from SENSOR_VP to SENSOR_CAPP.                             |
| SENSOR_CAPN | 7   | I    | GPIO38, SENSOR_CAPN, ADC1_CH2, ADC_PRE_AMP, RTC_GPIO2<br>Note: Connects 270pF capacitor from SENSOR_VN to SENSOR_CAPN.                             |
| SENSOR_VN   | 8   | I    | GPIO39, SENSOR_VN, ADC1_CH3, ADC_PRE_AMP, RTC_GPIO3<br>Note: Connects 270pF capacitor from SENSOR_VN to SENSOR_CAPN.                               |
| CHIP_PU     | 9   | I    | Chip Enable (Active High)<br>High: On, chip works properly<br>Low: Off, chip works at the minimum power<br>Note: Do not leave CHIP_PU pin floating |
| VDET_1      | 10  | I    | GPIO34, ADC1_CH6, RTC_GPIO4  |
| VDET_2      | 11  | I    | GPIO35, ADC1_CH7, RTC_GPIO5  |
| 32K_XP      | 12  | I/O  | GPIO32, 32K_XP (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9  |
| 32K_XN      | 13  | I/O  | GPIO33, 32K_XN (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8   |
| GPIO25      | 14  | I/O  | GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0  |
| GPIO26      | 15  | I/O  | GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1  |
| GPIO27      | 16  | I/O  | GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV   |
| MTMS        | 17  | I/O  | GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2  |
| MTDI        | 18  | I/O  | GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3  |
| VDD3P3_RTC  | 19  | P    | RTC IO power supply input (1.8V - 3.3V)  |
| MTCK        | 20  | I/O  | GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER   |
| MTDO        | 21  | I/O  | GPIO15, ADC2_CH3, TOUCH3, RTC_GPIO13, MTDO, HSPICS0, HS2_CMD, SD_CMD, EMAC_RXD3  |
| GPIO2       | 22  | I/O  | GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0   |
| GPIO0       | 23  | I/O  | GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK   |

| Name       | No. | Type | Function   |
|------------|-----|------|--|
| GPIO4      | 24  | I/O  | GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPiHD, HS2_DATA1, SD_DATA1, EMAC_TX_ER |
| GPIO16     | 25  | I/O  | GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT                                       |
| VDD_SDIO   | 26  | P    | 1.8V or 3.3V power supply output   |
| GPIO17     | 27  | I/O  | GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180                                   |
| SD_DATA_2  | 28  | I/O  | GPIO9, SD_DATA2, SPiHD, HS1_DATA2, U1RXD                                     |
| SD_DATA_3  | 29  | I/O  | GPIO10, SD_DATA3, SPiWP, HS1_DATA3, U1TXD                                    |
| SD_CMD     | 30  | I/O  | GPIO11, SD_CMD, SPiCS0, HS1_CMD, U1RTS                                       |
| SD_CLK     | 31  | I/O  | GPIO6, SD_CLK, SPiCLK, HS1_CLK, U1CTS  |
| SD_DATA_0  | 32  | I/O  | GPIO7, SD_DATA0, SPiQ, HS1_DATA0, U2RTS                                      |
| SD_DATA_1  | 33  | I/O  | GPIO8, SD_DATA1, SPiD, HS1_DATA1, U2CTS                                      |
| GPIO5      | 34  | I/O  | GPIO5, VSPiCS0, HS1_DATA6, EMAC_RX_CLK                                       |
| GPIO18     | 35  | I/O  | GPIO18, VSPiCLK, HS1_DATA7   |
| GPIO23     | 36  | I/O  | GPIO23, VSPiD, HS1_STROBE  |
| VDD3P3_CPU | 37  | P    | CPU IO power supply input (1.8V - 3.3V)                                      |
| GPIO19     | 38  | I/O  | GPIO19, VSPiQ, U0CTS, EMAC_TXD0  |
| GPIO22     | 39  | I/O  | GPIO22, VSPiWP, U0RTS, EMAC_TXD1   |
| U0RXD      | 40  | I/O  | GPIO3, U0RXD, CLK_OUT2   |
| U0TXD      | 41  | I/O  | GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2  |
| GPIO21     | 42  | I/O  | GPIO21, VSPiHD, EMAC_TX_EN   |
| VDDA       | 43  | I/O  | Analog power supply (2.3V - 3.6V).   |
| XTAL_N     | 44  | O    | External crystal output  |
| XTAL_P     | 45  | I    | External crystal input   |
| VDDA       | 46  | P    | Digital power supply for PLL (2.3V - 3.6V)                                   |
| CAP2       | 47  | I    | Connects with a 3nF capacitor and 20k resistor in parallel to CAP1           |
| CAP1       | 48  | I    | Connects with a 10nF series capacitor to ground                              |
| VDDA2      | -   | P    | Second digital power supply (2.3V - 3.6V)                                    |
| RES_14K    | -   | I    | Connects with a 14k series resistor to ground                                |
| CAP_10N    | -   | I    | Connects with a 10nF series capacitor to ground                              |

## 3. Functional Description

This chapter describes the functions implemented in ESP32.

### 3.1 Block Diagram

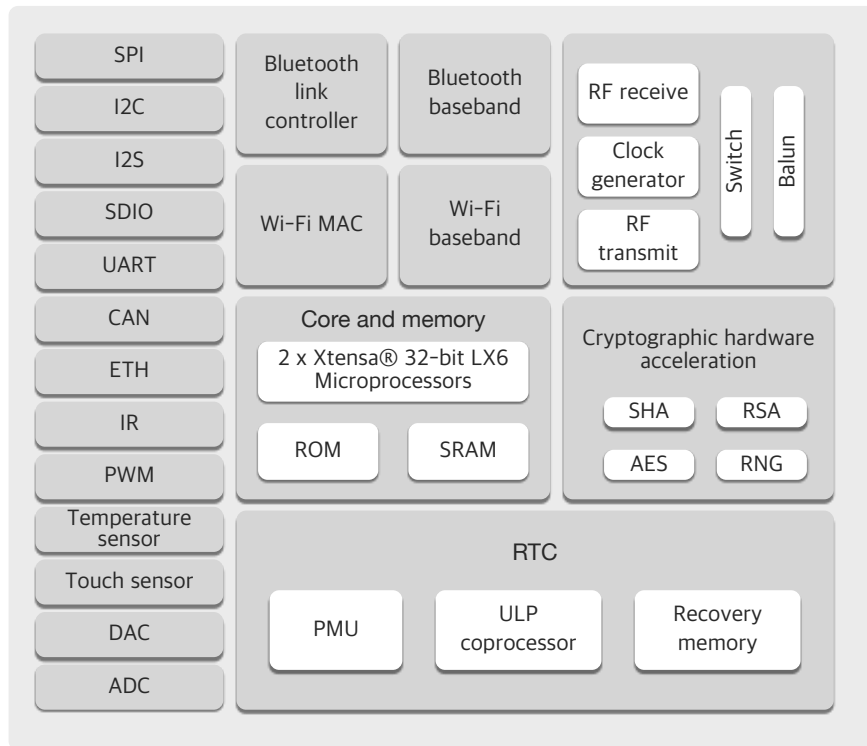


Figure 2: Function Block Diagram

### 3.2 Power Scheme

ESP32 digital pads are divided into three different power domains (see Table 1).

- VDD3P3\_RTC
- VDD3P3\_CPU
- VDD\_SDIO

**VDD3P3\_RTC** is also the input power supply for RTC and **VDD3P3\_CPU** is also the input power supply for CPU. **VDD\_SDIO** connects to the output of an internal LDO, whose input is **VDD3P3\_RTC**. When **VDD\_SDIO** is connected to the same PCB net together with **VDD3P3\_RTC**; the internal LDO is disabled automatically.

The internal LDO can be configured as 1.8V, or the same voltage as **VDD3P3\_RTC**. It can be powered off via software to minimize the current of flash during the deep sleep mode.



**Note:**

It is required that the power supply of **VDD3P3\_RTC**, **VDD3P3\_CPU** and analog keeping stable before the pin **CHIP\_EN** is set at high level.

### 3.3 Boot Modes Configuration

ESP32's strapping pins are sampled during system reset. During power on, the internal and external pull-up/pull-down resistors on strapping pins configure the device boot mode and the operating voltage of VDD\_SDIO. Please refer to Table 2 for detailed boot modes configuration by strapping pins.

Table 2: Strapping Pin List

| Voltage of Internal LDO (VDD_SDIO) |           |            |               |
|------------------------------------|-----------|------------|---------------|
| Pin                                | Default   | 3.3V       | 1.8V          |
| MTDI                               | Pull-down | 0          | 1             |
| Bootting Strapping Configuration   |           |            |               |
| Pin                                | Internal  | SPI Boot   | Download Boot |
| GPIO0                              | Pull-up   | 1          | 0             |
| U0TXD                              | Pull-up   | 1          | Don't-care    |
| GPIO2                              | Pull-down | Don't-care | 0             |
| GPIO4                              | Pull-down | Don't-care | Don't-care    |
| MTDO                               | Pull-up   | Don't-care | Don't-care    |
| GPIO5                              | Pull-up   | 1          | Don't-care    |

For example, if U0TXD, GPIO2, and GPIO5 are floating, then GPIO0 determines which boot mode to use.

- If GPIO0 is "1", the device switches to SPI Boot mode.
- If GPIO0 is "0", the device switches to Download Boot mode.

## 3.4 CPU, Flash and Memory

### 3.4.1 CPU

ESP32 contains two low-power Xtensa® 32-bit LX6 microprocessors with the following features.

- 7-stage pipeline to support the clock frequency of 160 MHz.
- 16/24-bit Instruction Set provides high code-density.
- Support Floating Point Unit.
- Support DSP instructions, such as 32-bit Multiplier, 32-bit Divider, and 40-bit MAC.
- Support 32 interrupt vectors from about 80 interrupt sources.

The dual CPUs interface through:

- Xtensa RAM/ROM Interface for instruction and data.
- Xtensa Local Memory Interface for fast register access.

- Processor Interface (PIF) with AHB-Lite bus bridge to access peripheral controllers.
- Interrupt with external and internal sources.
- JTAG interface for debugging.

### 3.4.2 Internal Memory

ESP32's internal memory includes:

- 128 kBytes ROM for booting and core functions. The two cores have dedicated ROM blocks.
- 512 kBytes on-chip SRAM which is split into 13 blocks of 32 kBytes. Each block of SRAM has an arbiter to mitigate the access conflicts between different CPUs and AHB buses.
- 8 kBytes SRAM in RTC, which is called recovery memory and can be used for data storage during the deep sleep mode.
- 1 kbit of EFUSE, of which 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including Flash-Encryption and Chip-ID.

### 3.4.3 External Flash and SRAM

ESP32 supports 4 x 16 MBytes of external QSPI flash and SRAM with hardware encryption based on AES-256 to protect developer's programs and data.

ESP32 accesses external QSPI flash and SRAM by the high-speed caches. Up to 8 MBytes of external flash are memory mapped into the CPU code space, supporting 8, 16 and 32-bit access. Code execution is supported. Up to 1 MByte of external flash and SRAM are memory mapped into the CPU data space, supporting 8, 16 and 32-bit access. Data read is supported on the flash and SRAM. Data read/write is supported on the SRAM.

### 3.4.4 Memory Map

The memory and register maps of ESP32 is shown in Table 3.

Table 3: Memory and Register Maps

| Blocks       | Description   | Start Address | Alternative Start Address | Size (Byte) |
|--------------|---------------|---------------|---------------------------|-------------|
| IROM         | -             | 0x40000000    | -                         | 64k         |
| IRAM         | -             | 0x40040000    | -                         | 128k        |
| DRAM         | -             | 0x3FFD8000    | -                         | 160k        |
| ICACHE       | -             | 0x40080000    | -                         | 3.5M        |
| DCACHE       | -             | 0x3FE00000    | -                         | 512k        |
| RTC Memory   | -             | 0x60021000    | 0x3FF61000                | 8k          |
| UART_BASE    | UART0         | 0x60000000    | -                         | 4k Space    |
| HSPI_BASE    | HSPI (SPI2)   | 0x60002000    | 0x3FF42000                | 4k Space    |
| SPI_BASE     | SPI (SPI1)    | 0x60003000    | 0x3FF43000                | 4k Space    |
| GPIO_BASE    | -             | 0x60004000    | 0x3FF44000                | 4k Space    |
| TIMERS_BASE  | Legacy Timers | 0x60007000    | 0x3FF47000                | 4k Space    |
| RTCCNTL_BASE | RTC registers | 0x60008000    | 0x3FF48000                | 4k Space    |
| RTCIO_BASE   | RTC IO Mux    | 0x60008400    | 0x3FF48400                | 4k Space    |
| IO_MUX_BASE  | Main IO Mux   | 0x60009000    | 0x3FF49000                | 4k Space    |

| Blocks           | Description       | Start Address | Alternative Start Address | Size (Byte) |
|------------------|-------------------|---------------|---------------------------|-------------|
| WDG_BASE         | Legacy Watchdog   | 0x6000A000    | 0x3FF4A000                | 4k Space    |
| UHCI1_BASE       | UART1 DMA         | 0x6000C000    | 0x3FF4C000                | 4k Space    |
| I2S_BASE         | I2S               | 0x6000F000    | -                         | 4k Space    |
| UART1_BASE       | UART1             | 0x60010000    | -                         | 4k Space    |
| UHCIO_BASE       | UART0 DMA         | 0x60014000    | 0x3FF54000                | 4k Space    |
| RMT_BASE         | Remote Controll   | 0x60016000    | 0x3FF56000                | 4k Space    |
| PCNT_BASE        | Pulse Counter     | 0x60017000    | 0x3FF57000                | 4k Space    |
| LEDC_BASE        | LED PWM           | 0x60019000    | 0x3FF59000                | 4k Space    |
| EFUSE_BASE       | Efuse             | 0x6001A000    | 0x3FF5A000                | 4k Space    |
| PWM_BASE         | Motor PWM         | 0x6001C000    | 0x3FF5C000                | 4k Space    |
| TIMERGROUP_BASE  | Timer Group1      | 0x6001D000    | 0x3FF5D000                | 4k Space    |
| TIMERGROUP1_BASE | Timer Group1      | 0x6001E000    | 0x3FF5E000                | 4k Space    |
| PRO_DPORT        | CPU configuration | -             | 0x3FF00000                | 4k Space    |
| SDHOST_BASE      | SD/SDIO Host      | 0x61000000    | -                         | 1M Space    |

## 3.5 Timers and Watchdogs

### 3.5.1 Timers

There are three types of timers in ESP32.

- CPU internal timers: There are three timers in each CPU core. These timers are all 32-bit free-running counters. A target value can be programmed to trigger an interrupt.
- General-purpose timers: ESP32 includes 2 sets of 64-bit timers and 4 sets of 32-bit timers which can be configured to operate independently as follows:
  - Count up and reach the target value to generate a one-shot interrupt.
  - Count down and auto-reload to generate periodic interrupts.
  - 8-bit prescaler.
- RTC timer: The RTC integrates a free-running low-power 48-bit counter. This counter is started upon power-on. The user can configure a target value for the counter to generate a wake-up or interrupt signal.
  - This counter can be used to implement anti-rollback.

### 3.5.2 Watchdogs

The watchdog timer is used to re-assert control of the system when the system fails due to software errors or failure of external devices. ESP32 has three hardware watchdogs — two system watchdogs and an RTC watchdog. The system watchdogs run on the AHP clock (usually 80 MHz), while the RTC watchdog runs on the RTC clock (usually 32 kHz - 100 kHz). These three watchdogs have the following features:

- 32-bit down counter with a programmable load register.
- Lock register: Once the watchdog timer has been configured, the lock register can be written to prevent the timer configuration from being inadvertently altered.

- Three configurable stages: The watchdog timer can be configured to generate an interrupt to the CPUs on its first time-out, to generate a local reset signal on its second time-out, and to generate a global reset signal on its third time-out. The local reset signal is used to reset one or both of the CPU cores. The global reset signal will reboot the whole system.
- Boot up: One of the system watchdogs and the RTC watchdog are enabled on the 3rd stage by default. If the boot process from an SPI flash does not complete within a predetermined time period, the watchdog will reboot the whole system.

## 3.6 Clock

### 3.6.1 CPU Clock

Upon reset, an external crystal clock source (20 MHz - 60 MHz), after division by 2, is selected as the default CPU clock. The external crystal clock source also connects to a PLL to generate a high frequency clock (typically about 160 MHz).

In addition to this, ESP32 has an internal 8 MHz oscillator, of which the accuracy is guaranteed by design and is stable over temperature (within 1% accuracy). Hence, the application can then select from the external crystal clock source, the PLL clock or the internal 8 MHz oscillator. The selected clock source drives the CPU clock, directly or after division, depending on the application.

### 3.6.2 RTC Clock

The RTC clock has five possible sources:

- external low speed (32 kHz) crystal clock,
- external crystal clock divided by 4,
- internal RC oscillator (typically about 150 kHz and adjustable),
- internal 8 MHz oscillator, and
- internal 31.25 kHz clock (derived from the internal 8 MHz oscillator divided by 256).

When the chip is in the normal power mode and needs a faster CPU clock, the application can choose the external high speed crystal clock divided by 4 or the internal 8 MHz oscillator. When the chip operates in the low power mode, the application chooses the external low speed (32 kHz) crystal clock, the internal RC oscillator, the internal 8 MHz oscillator or the internal 31.25 kHz clock.

### 3.6.3 Audio PLL Clock

The audio clock is generated by the ultra low noise fractional-N PLL. The output frequency of the audio PLL is programmable, from 16 MHz to 128 MHz, given by the following formula:

$$f_{out} = \frac{f_{xtal} N_{div}}{M_{div} 2^{K_{div}}}$$

where  $f_{out}$  is the output frequency,  $f_{xtal}$  is the frequency of the crystal oscillator, and  $N_{div}$ ,  $M_{div}$  and  $K_{div}$  are all integer values, configurable by registers.

## 3.7 Radio

The ESP32 radio consists of the following main blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

### 3.7.1 2.4 GHz Receiver

The 2.4 GHz receiver down-converts the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with 2 high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits and baseband filters are integrated within ESP32.

### 3.7.2 2.4 GHz Transmitter

The 2.4 GHz transmitter up-converts the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high powered Complementary Metal Oxide Semiconductor (CMOS) power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling state-of-the-art performance of delivering +20.5 dBm of average power for 802.11b transmission and +17 dBm for 802.11n transmission.

Additional calibrations are integrated to cancel any imperfections of the radio, such as:

- Carrier leakage
- I/Q phase matching
- Baseband nonlinearities
- RF nonlinearities
- Antenna matching

These built-in calibration routines reduce the amount of time and required for product test and make test equipments unnecessary.

### 3.7.3 Clock Generator

The clock generator generates quadrature 2.4 GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on the chip, including all inductors, varactors, filters, regulators and dividers. The clock generator has built-in calibration and self test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best performance of the receiver and transmitter.

## 3.8 Bluetooth

ESP32 integrates Bluetooth link controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packets processing, bit stream processing, frequency hopping, etc.

### 3.8.1 Radio

- Supports class-1, class-2 and class-3 transmit output powers and over 30dB dynamic control range.
- Supports  $\pi/4$  DQPSK and 8 DPSK modulation.
- High performance in receiver sensitivity with over 90dB dynamic range.
- Supports class-1 operation without external PA.

### 3.8.2 Baseband

- Internal SRAM allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- Supports ACL, SCO, eSCO and AFH
- Supports A-law,  $\mu$ -law and CVSD digital audio CODEC in PCM interface
- Supports SBC audio CODEC
- Supports power management for low power applications
- Supports SMP with 128-bit AES

### 3.8.3 Interface

- Provides UART HCI interface, up to 4 Mbps
- Provides SDIO / SPI HCI interface
- Provides I2C interface for the host to do configuration
- Provides PCM / I2S audio interface

### 3.8.4 Bluetooth Stack

Compliant with Bluetooth v4.2 BR / EDR and BLE specification

## 3.9 Wi-Fi

ESP32 implements TCP/IP, full 802.11 b/g/n/e/i WLAN MAC protocol, and Wi-Fi Direct specification. It supports Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF) and P2P group operation compliant with the latest Wi-Fi P2P protocol.

ESP32 applies low level protocol functions automatically as follows:

- Request To Send (RTS) / Clear To Send (CTS)
- Acknowledgement
- Fragmentation and defragmentation
- Aggregation
- Frame encapsulation (802.11h / RFC 1042)
- Automatic beacon monitoring / scanning
- P2P Wi-Fi Direct

Passive or active scanning, as well as the P2P discovery procedure are performed autonomously when initiated by appropriate commands. Power management is handled with minimum host interaction to minimize active duty period.

### 3.9.1 Wi-Fi Radio and Baseband

The ESP32 Wi-Fi Radio and Baseband support the following features:

- 802.11b and 802.11g data-rates
- 802.11n MCS0-7 in both 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- .11n 0.4  $\mu$ S guard-interval
- Data-rate up to 150 Mbps
- Receiving STBC 2x1
- Up to 21 dBm transmitting power
- Adjustable transmitting power
- Antenna diversity and selection (software managed hardware)

### 3.9.2 Wi-Fi MAC

The ESP32 Wi-Fi MAC applies low level protocol functions automatically as follows:

- Request To Send (RTS), Clear To Send (CTS) and Acknowledgement (ACK/BA)
- Fragmentation and defragmentation
- Aggregation AMPDU and AMSDU
- WMM power save U-APSD
- Multiple transmitting queue management to fully utilize QoS traffic prioritization defined by 802.11e standard
- CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4) and CRC
- Frame encapsulation (802.11h/RFC 1042)
- Automatic beacon monitoring/scanning

### 3.9.3 Wi-Fi Firmware

The ESP32 Wi-Fi Firmware provides the following functions:

- Infrastructure BSS Station mode/P2P mode/softAP mode support
- P2P Discovery, P2P Group Owner mode and P2P Power Management
- WPA/WPA2 PSK and WPS driver
- Additional 802.11i security features such as pre-authentication and TSN
- Open interface for various upper layer authentication schemes over EAP such as TLS, PEAP, LEAP, SIM, AKA or customer specific
- Clock/power gating combined with 802.11-compliant power management dynamically adapted to current connection condition providing minimal power consumption
- Adaptive rate fallback algorithm sets the optimal transmission rate and transmit power based on actual Signal Noise Ratio (SNR) and packet loss information
- Automatic retransmission and response on MAC to avoid packet discarding on slow host environment

### 3.9.4 Packet Traffic Arbitration (PTA)

ESP32 has a configurable Packet Traffic Arbitration (PTA) that provides flexible and exact timing Bluetooth co-existence support. It is a combination of both Frequency Division Multiplexing (FDM) and Time Division Multiplexing (TDM), and coordinates the protocol stacks.

- It is preferable that Wi-Fi works in the 20 MHz bandwidth mode to decrease its interference with BT.
- BT applies AFH (Adaptive Frequency Hopping) to avoid using the channels within Wi-Fi bandwidth.
- Wi-Fi MAC limits the time duration of Wi-Fi packets, and does not transmit the long Wi-Fi packets by the lowest data-rates.
- Normally BT packets are of higher priority than normal Wi-Fi packets.
- Protect the critical Wi-Fi packets, including beacon transmission and receiving, ACK/BA transmission and receiving.
- Protect the highest BT packets, including inquiry response, page response, LMP data and response, park beacons, the last poll period, SCO/eSCO slots, BLE event sequence.
- Wi-Fi MAC apply CTS-to-self packet to protect the time duration of BT transfer.
- In the P2P Group Own (GO) mode, Wi-Fi MAC applies a Notice of Absence (NoA) packet to disable Wi-Fi transfer to reserve time for BT.
- In the STA Mode, Wi-Fi MAC applies a NULL packet with the Power-Save bit to disable WiFi transfer to reserve time for BT.

## 3.10 Low-Power Management

With the advanced power management technologies, ESP32 can switch between different power modes (see Table 4).

- Power mode



- Shutdown (Turn-off): RTC is disabled and all registers are cleared. The chip is totally powered down.
  - Active mode: In the active mode, the chip radio is powered on. The chip can receive, transmit, or listen.
  - Modem sleep mode: In the modem sleep mode, the CPU is operational and the clock is configurable. The Wi-Fi/Bluetooth baseband and radio are disabled.
  - Light sleep mode: The CPU is paused in the light sleep mode. The RTC and ULP-coprocessor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.
  - Deep sleep mode: Only RTC is powered on. Wi-Fi and Bluetooth connection data are stored in RTC memory. The ULP-coprocessor can work.
- Sleep Pattern
    - Association sleep pattern: The power mode switches between the active mode and light sleep mode during this sleep pattern. The CPU, Wi-Fi, Bluetooth, and radio are woken up at predetermined intervals to keep Wi-Fi/BT connections alive.
    - Sensor-monitored deep sleep pattern: The ULP co-processor is enabled or disabled at intervals depending on the measured data from sensors.

Table 4: Functionalities Depending on the Power Modes

| Power mode                    | Active mode       | Light sleep | Modem sleep                 | Deep sleep | Shutdown (Turn-off) |
|-------------------------------|-------------------|-------------|-----------------------------|------------|---------------------|
| Sleep pattern                 | Association sleep |             | Sensor-monitored deep sleep |            |                     |
| CPU                           | ON                | PAUSE       | ON                          | OFF        | OFF                 |
| Wi-Fi / BT baseband and radio | ON                | OFF         | OFF                         | OFF        | OFF                 |
| RTC                           | ON                | ON          | ON                          | ON         | OFF                 |
| ULP coprocessor               | ON                | ON          | ON                          | ON/OFF     | OFF                 |

The power consumption varies with different power modes/sleep patterns and work status of functional modules (see Table 5).

Table 5: Power Consumption by Power Modes

| Power mode               | Comment                                    | Power consumption                                      |
|--------------------------|--|--|
| Active mode (RF working) | Wi-Fi Tx packet 13 dBm - 21 dBm            | 160 - 260 mA   |
|                          | Wi-Fi / BT Tx packet 0 dBm                 | 120 mA   |
|                          | Wi-Fi / BT Rx and listening                | 80 - 90 mA   |
|                          | Association sleep pattern (by light sleep) | 0.9 mA@DTIM3 1.2 mA@DTIM1                              |
| Modem sleep              | The CPU is powered on                      | Max speed: 20 mA Normal: 5 - 10 mA<br>Slow speed: 3 mA |
| Light sleep              | -  | 0.8 mA   |
| Deep sleep               | The ULP-coprocessor is powered on          | 0.5 mA   |
|                          | Sensor-monitored deep sleep pattern        | 25 $\mu$ A @1% duty                                    |
|                          | RTC timer + recovery-memory                | 20 $\mu$ A   |
|                          | RTC timer only                             | 5 $\mu$ A  |

| Power mode          | Comment | Power consumption |
|---------------------|---------|-------------------|
| Shutdown (Turn-off) | -       | 2 $\mu$ A         |

**Note:**

For more information about RF power consumption, please refer to Section [5.3 RF Power Consumption Specifications](#).

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## 4. Peripheral Interface

### 4.1 General Purpose Input / Output Interface (GPIO)

ESP32 has 36 GPIO pins which can be assigned to various functions by programming the appropriate registers. There are several kinds of GPIOs: digital only GPIOs, analog enabled GPIOs, capacitive touch enabled GPIOs, etc. Analog enabled GPIOs can be configured as digital GPIOs. Capacitive touch enabled GPIOs can be configured as digital GPIOs.

Each digital enabled GPIO can be configured to internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. In short, the digital IO pads are bi-directional, non-inverting and tristate, including input and output buffer with tristate control.

These pins can be multiplexed with other functions, such as the SDIO interface, UART, SI, etc. For low power operations, the GPIOs can be set to hold their states.

### 4.2 Analog-to-Digital Converter (ADC)

ESP32 integrates 12-bit SAR ADCs and supports measurements on 16 channels (analog enabled pads). Some of these pads can be used to build a programmable gain amplifier which is used for the measurement of small analog signals. The ULP-coprocessor in ESP32 is also designed to measure the voltages while operating in the sleep mode, to enable low power consumption; the CPU can be woken up by a threshold setting and/or via other triggers.

With the appropriate setting, the ADCs and the amplifier can be configured to measure voltages for a maximum of 16 pads.

### 4.3 Ultra Low Noise Analog Pre-Amplifier

ESP32 integrates an ultra low noise analog pre-amplifier that outputs to the ADC. The amplification ratio is given by the size of a pair of sampling capacitors that are placed off-chip. By using a larger capacitor, the sampling noise is reduced, but the settling time will be increased. The amplification ratio is also limited by the amplifier which peaks at about 60dB gain.

### 4.4 Hall Sensor

ESP32 integrates a Hall sensor that outputs to the ADC. The Hall sensor is based on an N-carrier resistor; when a current flows in the presence of a magnetic field, it develops a small voltage laterally on the resistor, which can be amplified by a low-power, ultra low noise amplifier and measured by the ADC.

### 4.5 Digital-to-Analog Converter (DAC)

Two 8-bit DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The design structure is composed of integrated resistor strings and a buffer. This dual DAC supports input voltage reference power supply and dual channel independent or simultaneous conversions.

## 4.6 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an analog-to-digital converter into a digital code.

The temperature sensor has a range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . As the offset of the temperature sensor varies from chip to chip due to process variation, and due to the heat generated by the Wi-Fi circuitry itself (which affects measurements), the internal temperature sensor is only suitable for applications that detect temperature changes instead of absolute temperatures and for calibration purposes as well.

However, if the user calibrates the temperature sensor and uses the device in a minimally powered-on application, the results could be accurate enough.

## 4.7 Touch Sensor

ESP32 offers 10 capacitive sensing GPIOs which detect capacitive variations introduced by the GPIO's direct contact or close proximity with a finger or other objects. The low noise nature of the design and high sensitivity of the circuit allows relatively small pads to be used. Arrays of pads can also be used so that a larger area or more points can be detected. The 10 capacitive sensing GPIOs are listed in Table 6.

Table 6: Capacitive Sensing GPIOs Available on ESP32

| Capacitive sensing signal name | Pin name |
|--------------------------------|----------|
| T0                             | GPIO4    |
| T1                             | GPIO0    |
| T2                             | GPIO2    |
| T3                             | MTDO     |
| T4                             | MTCK     |
| T5                             | MTD1     |
| T6                             | MTMS     |
| T7                             | GPIO27   |
| T8                             | 32K_XN   |
| T9                             | 32K_XP   |

**Note:**

For more information about the touch sensor design and layout, please refer to Chapter 8 Touch Sensor.

## 4.8 Ultra-Lower-Power Coprocessor

The ULP processor and RTC memory remains powered on during DeepSleep. Hence, the developer can store a program for the ULP processor in the RTC memory to access the peripheral devices, internal timers and internal sensors during deep sleep. This is useful for designing applications where the CPU needs to be woken up by an external event, or timer, or a combination of these events, while maintaining minimal power consumption.

## 4.9 Ethernet MAC Interface

An IEEE-802.3-2008-compliant Media Access Controller (MAC) is provided for Ethernet LAN communications. ESP32 requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to ESP32 through 17 signals of MII, 9 signals of RMII, 6 signals of SMII or 8 signals of SS-SMII. With the Ethernet MAC interface, the following features are supported:

- 10 Mbps and 100 Mbps rates
- Dedicated DMA controller allowing high-speed transfer between the dedicated SRAM and the descriptors
- Tagged MAC frame (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 256 bytes
- Hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2)
- 25 MHz/50 MHz clock output

## 4.10 SD / SDIO / MMC Host Controller

An SD/SDIO/MMC host controller is available on ESP32, and it supports:

- Secure Digital memory (SD mem Version 3.0 and Version 3.01)
- Secure Digital I/O (SDIO Version 3.0)
- Consumer Electronics Advanced Transport Architecture (CE-ATA Version 1.1)
- Multimedia Cards (MMC Version 4.41, eMMC Version 4.5 and Version 4.51)

The controller allows data transfer at up to 80 MHz and in three different data-bus modes: 1-bit, 4-bit and 8-bit. It supports two SD/SDIO/MMC4.41 cards in 4-bit data-bus mode. It also supports one SD card operating at 1.8V level.

## 4.11 Universal Asynchronous Receiver Transmitter (UART)

ESP32 has two UART interfaces, i.e. UART0 and UART1, which provide asynchronous communication (RS232 and RS485) and IrDA support, and communicate at up to 5 Mbps. UART provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). Both of the interfaces can be accessed by the DMA controller or directly by CPU.

## 4.12 I2C Interface

ESP32 has two I2C bus interfaces which can serve as I2C master or slave depending on the user's configuration. The I2C interfaces support:

- Standard mode (100 kbit/s)
- Fast mode (400 kbit/s)
- Up to 5 MHz, but constrained by SDA pull up strength
- 7/10-bit addressing mode
- 7-bit dual addressing mode

Users can program command registers to control I2C interfaces to have more flexibility. TXFIFO and RXFIFO are used to support multiple commands at a time.

## 4.13 I2S Interface

Two standard I2S interfaces are available in ESP32. They can be operated in the master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with an 8-/16-/32-/40-/48-bit resolution as input or output channels. BCK clock frequency from 10 kHz up to 40 MHz are supported. When one or both of the I2S interfaces are configured in the master mode, the master clock can be output to the external DAC / CODEC at 64 times the sampling frequency.

Both of the I2S interfaces have dedicated DMA controllers. PDM and BT PCM interfaces are supported.

## 4.14 Infrared Remote Controller

The infrared remote controller supports eight channels of infrared remote transmission and receiving. Through programming the pulse waveform, it supports various infrared protocols. Eight channels share a 512 x 32-bit block of memory to store the transmitting or receiving waveform.

## 4.15 Pulse Counter

The pulse counter captures pulse and counts pulse edges through seven modes. It captures four groups at a time. The input in each group includes two pulse signals and two control signals. When the counter reaches a defined threshold, an interrupt is generated.

## 4.16 Pulse Width Modulation

The Pulse Width Modulation (PWM) controller can be used for driving digital motors and smart lights. The controller consists of PWM timers, PWM sub-controllers and a dedicated capture sub-module. Each timer provides timing in synced or free-run form, and each PWM sub-controller generates the waveform for one PWM channel. The dedicated sub-module can accurately capture external timing events.

## 4.17 LED PWM

The LED PWM controller can generate 16 independent channels of digital waveforms with the configurable periods and configurable duties.

Each channel houses a 20-bit timer running at 80 MHz. For each 20-bit timer, a 20-bit register configures the period, and the other two 20-bit registers determine the rising and falling edge of the pulse. Therefore, the period of the PWM can be configured from 1/80 s to 1/40  $\mu$ s, and the accuracy of the duty can be up to 16-bit with the 1ms period.

The software can change the duty immediately. Moreover, each channel supports step-by-step duty increasing or decreasing automatically. It is useful for the LED RGB color gradient generator.

## 4.18 Serial Peripheral Interface (SPI)

ESP32 features three SPIs (SPI, HSPI and VSPI) in slave and master modes in 1-line full-duplex and 1/2/4-line simplex communication modes. These SPIs also support:

- 4 timing modes of the SPI format transfer that depend on the polarity (POL) and the phase (PHA)
- up to 80 MHz and the divided clocks of 80 MHz
- up to 64 Byte FIFO

This interface can be used to connect to the external flash / SRAM and LCD. All SPIs can be served by the DMA controller.

## 5. Electrical Specifications

### Note:

The specifications in this chapter are tested in general condition: VBAT = 3.3V, TA = 27°C, unless otherwise specified.

### 5.1 DC Electrical Characteristics

#### 5.1.1 Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

| Parameter                 | Symbol    | Min                  | Max                  | Unit |
|---------------------------|-----------|----------------------|----------------------|------|
| Input low voltage         | $V_{IL}$  | -0.3                 | $0.25 \times V_{IO}$ | V    |
| Input high voltage        | $V_{IH}$  | $0.75 \times V_{IO}$ | 3.3                  | V    |
| Input leakage current     | $I_{IL}$  | -                    | 50                   | nA   |
| Output low voltage        | $V_{OL}$  | -                    | $0.1 \times V_{IO}$  | V    |
| Output high voltage       | $V_{OH}$  | $0.8 \times V_{IO}$  | -                    | V    |
| Input pin capacitance     | $C_{pad}$ | -                    | 2                    | pF   |
| VDDIO                     | $V_{IO}$  | 1.8                  | 3.3                  | V    |
| Maximum drive capability  | $I_{MAX}$ | -                    | 12                   | mA   |
| Storage temperature range | $T_{STR}$ | -40                  | 150                  | °C   |

### 5.2 Recommended Operating Conditions

Table 8: Recommended Operating Conditions

| Parameter                        | Symbol | Min                 | Typ                 | Max                 | Unit |
|----------------------------------|--------|---------------------|---------------------|---------------------|------|
| Battery regulator supply voltage | VBAT   | 2.8                 | 3.3                 | 3.6                 | V    |
| I/O supply voltage               | VIO    | 1.8                 | 3.3                 | 3.6                 | V    |
| Operating temperature range      | TOPR   | -40                 | -                   | 125                 | °C   |
| CMOS low level input voltage     | VIL    | 0                   | -                   | $0.3 \times V_{IO}$ | V    |
| CMOS high level input voltage    | VIH    | $0.7 \times V_{IO}$ | -                   | $V_{IO}$            | V    |
| CMOS threshold voltage           | VTH    | -                   | $0.5 \times V_{IO}$ | -                   | V    |

### 5.3 RF Power Consumption Specifications

The current consumption measurements are conducted with 3.0V supply and 25°C ambient, at antenna port. All the transmitters' measurements are based on 90% duty cycle and continuous transmit mode.

Table 9: RF Power Consumption Specifications

| Mode  | Min | Typ | Max | Unit |
|---|-----|-----|-----|------|
| Transmit 802.11b, DSSS 1 Mbps, POUT=+19.5 dBm | -   | 225 | -   | mA   |
| Transmit 802.11b, CCK 11 Mbps, POUT=+18.5 dBm | -   | 205 | -   | mA   |
| Transmit 802.11g, OFDM 54 Mbps, POUT=+16 dBm  | -   | 160 | -   | mA   |



| Mode  | Min | Typ | Max | Unit |
|---|-----|-----|-----|------|
| Transmit 802.11n, MCS7, POUT=+14 dBm                    | -   | 152 | -   | mA   |
| Receive 802.11b, packet length=1024 bytes, -80 dBm      | -   | 85  | -   | mA   |
| Receive 802.11g, packet length=1024 bytes, -70 dBm      | -   | 85  | -   | mA   |
| Receive 802.11n, packet length=1024 bytes, -65 dBm      | -   | 80  | -   | mA   |
| Receive 802.11n HT40, packet length=1024 bytes, -65 dBm | -   | 80  | -   | mA   |

## 5.4 Bluetooth Radio

### 5.4.1 Receiver - Basic Data Rate

Table 10: Receiver Characteristics-Basic Data Rate

| Parameter                         | Conditions          | Min | Typ | Max | Unit |
|-----------------------------------|---------------------|-----|-----|-----|------|
| Sensitivity @0.1% BER             | -                   | -   | -90 | -   | dBm  |
| Maximum received signal @0.1% BER | -                   | 0   | -   | -   | dBm  |
| Co-channel C/I                    | -                   | -   | +7  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 1 MHz        | -   | -   | -6  | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 1 MHz        | -   | -   | -6  | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 2 MHz        | -   | -   | -33 | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 2 MHz        | -   | -   | -25 | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 3 MHz        | -   | -   | -45 | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 3 MHz        | -   | -   | -25 | dB   |
| Out-of-band blocking performance  | 30 MHz - 2000 MHz   | -10 | -   | -   | dBm  |
| Out-of-band blocking performance  | 2000 MHz - 2400 MHz | -27 | -   | -   | dBm  |
| Out-of-band blocking performance  | 2500 MHz - 3000 MHz | -27 | -   | -   | dBm  |
| Out-of-band blocking performance  | 3000 MHz - 12.5 GHz | -10 | -   | -   | dBm  |
| Intermodulation                   | -                   | -36 | -   | -   | dBm  |

### 5.4.2 Transmit - Basic Data Rate

Table 11: Transmit Characteristics - Basic Data Rate

| Parameter                       | Conditions    | Min | Typ   | Max | Unit |
|---------------------------------|---------------|-----|-------|-----|------|
| RF transmit power               | -             | -   | +4    | +4  | dBm  |
| RF power control range          | -             | -   | 25    | -   | dB   |
| 20 dB bandwidth                 | -             | -   | 0.9   | -   | MHz  |
| Adjacent channel transmit power | F=F0 + 1 MHz  | -   | -24   | -   | dBm  |
| Adjacent channel transmit power | F=F0 - 1 MHz  | -   | -16.1 | -   | dBm  |
| Adjacent channel transmit power | F=F0 + 2 MHz  | -   | -40.8 | -   | dBm  |
| Adjacent channel transmit power | F=F0 - 2 MHz  | -   | -35.6 | -   | dBm  |
| Adjacent channel transmit power | F=F0 + 3 MHz  | -   | -45.7 | -   | dBm  |
| Adjacent channel transmit power | F=F0 - 3 MHz  | -   | -40.2 | -   | dBm  |
| Adjacent channel transmit power | F=F0 + >3 MHz | -   | -45.6 | -   | dBm  |
| Adjacent channel transmit power | F=F0 - >3 MHz | -   | -44.6 | -   | dBm  |

| Parameter                               | Conditions | Min | Typ   | Max | Unit           |
|---|------------|-----|-------|-----|----------------|
| $\Delta f_{1_{avg}}$ Maximum modulation | -          | -   | 155   | -   | kHz            |
| $\Delta f_{2_{max}}$ Minimum modulation | -          | -   | 133.7 | -   | kHz            |
| $\Delta f_{2_{avg}}/\Delta f_{1_{avg}}$ | -          | -   | 0.92  | -   | -              |
| ICFT                                    | -          | -   | -7    | -   | kHz            |
| Drift rate                              | -          | -   | 0.7   | -   | kHz/50 $\mu$ s |
| Drift (1 slot packet)                   | -          | -   | 6     | -   | kHz            |
| Drift (5 slot packet)                   | -          | -   | 6     | -   | kHz            |

### 5.4.3 Receiver - Enhanced Data Rate

Table 12: Receiver Characteristics - Enhanced Data Rate

| Parameter                         | Conditions   | Min | Typ | Max | Unit |
|-----------------------------------|--------------|-----|-----|-----|------|
| $\pi/4$ DQPSK                     |              |     |     |     |      |
| Sensitivity @0.01% BER            | -            | -   | -91 | -   | dBm  |
| Maximum received signal @0.1% BER | -            | -   | 0   | -   | dBm  |
| C/I c-channel                     | -            | -   | 11  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 1 MHz | -   | -7  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 1 MHz | -   | -7  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 2 MHz | -   | -35 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 2 MHz | -   | -25 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 3 MHz | -   | -45 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 3 MHz | -   | -25 | -   | dB   |
| DQPSK                             |              |     |     |     |      |
| Sensitivity @0.01% BER            | -            | -   | -84 | -   | dBm  |
| Maximum received signal @0.1% BER | -            | 0   | -   | -   | dBm  |
| C/I c-channel                     | -            | -   | 18  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 1 MHz | -   | 2   | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 1 MHz | -   | 2   | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 2 MHz | -   | -25 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 2 MHz | -   | -25 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 3 MHz | -   | -38 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 3 MHz | -   | -38 | -   | dB   |

### 5.4.4 Transmit - Enhanced Data Rate

Table 13: Transmit Characteristics - Enhanced Data Rate

| Parameter                  | Conditions | Min | Typ   | Max | Unit |
|----------------------------|------------|-----|-------|-----|------|
| Maximum RF transmit power  | -          | -   | +2    | -   | dBm  |
| Relative transmit control  | -          | -   | -1.5  | -   | dB   |
| $\pi/4$ DQPSK max w0       | -          | -   | -0.72 | -   | kHz  |
| $\pi/4$ DQPSK max wi       | -          | -   | -6    | -   | kHz  |
| $\pi/4$ DQPSK max  wi + w0 | -          | -   | -7.42 | -   | kHz  |

| Parameter                         | Conditions      | Min | Typ   | Max   | Unit |
|-----------------------------------|-----------------|-----|-------|-------|------|
| 8DPSK max w0                      | -               | -   | 0.7   | -     | kHz  |
| 8DPSK max wi                      | -               | -   | -9.6  | -     | kHz  |
| 8DPSK max  wi + w0                | -               | -   | -10   | -     | kHz  |
| $\pi/4$ DQPSK modulation accuracy | RMS DEVM        | -   | 4.28  | -     | %    |
| $\pi/4$ DQPSK modulation accuracy | 99% DEVM        | -   | -     | 30    | %    |
| $\pi/4$ DQPSK modulation accuracy | Peak DEVM       | -   | 13.3  | -     | %    |
| 8DPSK modulation accuracy         | RMS DEVM        | -   | 5.8   | -     | %    |
| 8DPSK modulation accuracy         | 99% DEVM        | -   | -     | 20    | %    |
| 8DPSK modulation accuracy         | Peak DEVM       | -   | 14    | -     | %    |
| In-band spurious emissions        | F=F0 + 1MHz     | -   | -34   | -     | dBm  |
| In-band spurious emissions        | F=F0 - 1MHz     | -   | -40.2 | -     | dBm  |
| In-band spurious emissions        | F=F0 + 2MHz     | -   | -34   | -     | dBm  |
| In-band spurious emissions        | F=F0 - 2MHz     | -   | -36   | -     | dBm  |
| In-band spurious emissions        | F=F0 + 3MHz     | -   | -38   | -     | dBm  |
| In-band spurious emissions        | F=F0 - 3MHz     | -   | -40.3 | -     | dBm  |
| In-band spurious emissions        | F=F0 +/- > 3MHz | -   | -     | -41.5 | dBm  |
| EDR differential phase coding     | -               | -   | 100   | -     | %    |

## 5.5 Bluetooth LE Radio

### 5.5.1 Receiver

Table 14: Receiver Characteristics - BLE

| Parameter                         | Conditions          | Min | Typ | Max | Unit |
|-----------------------------------|---------------------|-----|-----|-----|------|
| Sensitivity @0.1% BER             | -                   | -   | -92 | -   | dBm  |
| Maximum received signal @0.1% BER | -                   | 0   | -   | -   | dBm  |
| Co-channel C/I                    | -                   | -   | +10 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 1 MHz        | -   | -5  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 1 MHz        | -   | -5  | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 2 MHz        | -   | -35 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 2 MHz        | -   | -25 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 + 3 MHz        | -   | -45 | -   | dB   |
| Adjacent channel selectivity C/I  | F=F0 - 3 MHz        | -   | -25 | -   | dB   |
| Out-of-band blocking performance  | 30 MHz - 2000 MHz   | -10 | -   | -   | dBm  |
| Out-of-band blocking performance  | 2000 MHz - 2400 MHz | -27 | -   | -   | dBm  |
| Out-of-band blocking performance  | 2500 MHz - 3000 MHz | -27 | -   | -   | dBm  |
| Out-of-band blocking performance  | 3000 MHz - 12.5 GHz | -10 | -   | -   | dBm  |
| Intermodulation                   | -                   | -36 | -   | -   | dBm  |

### 5.5.2 Transmit

Table 15: Transmit Characteristics - BLE

| Parameter                               | Conditions     | Min | Typ   | Max | Unit              |
|---|----------------|-----|-------|-----|-------------------|
| RF transmit power                       | -              | -   | +7.5  | +10 | dBm               |
| RF power control range                  | -              | -   | 25    | -   | dB                |
| Adjacent channel transmit power         | F=F0 + 1 MHz   | -   | -14.6 | -   | dBm               |
| Adjacent channel transmit power         | F=F0 - 1 MHz   | -   | -12.7 | -   | dBm               |
| Adjacent channel transmit power         | F=F0 + 2 MHz   | -   | -44.3 | -   | dBm               |
| Adjacent channel transmit power         | F=F0 - 2 MHz   | -   | -38.7 | -   | dBm               |
| Adjacent channel transmit power         | F=F0 + 3 MHz   | -   | -49.2 | -   | dBm               |
| Adjacent channel transmit power         | F=F0 - 3 MHz   | -   | -44.7 | -   | dBm               |
| Adjacent channel transmit power         | F=F0 + > 3 MHz | -   | -50   | -   | dBm               |
| Adjacent channel transmit power         | F=F0 - > 3MHz  | -   | -50   | -   | dBm               |
| $\Delta f_{1_{avg}}$ Maximum modulation | -              | -   | 265   | -   | kHz               |
| $\Delta f_{2_{avg}}$ Maximum modulation | -              | -   | 247   | -   | kHz               |
| $\Delta f_{2_{avg}}/\Delta f_{1_{avg}}$ | -              | -   | -0.92 | -   | -                 |
| ICFT                                    | -              | -   | -10   | -   | kHz               |
| Drift rate                              | -              | -   | 0.7   | -   | kHz/50<br>$\mu$ s |
| Drift                                   | -              | -   | 2     | -   | kHz               |

## 5.6 Wi-Fi Radio

Table 16: Wi-Fi Radio Characteristics

| Description                      | Min  | Typical | Max  | Unit |
|----------------------------------|------|---------|------|------|
| Input frequency                  | 2412 | -       | 2484 | MHz  |
| Input impedance                  | -    | 50      | -    |      |
| Input reflection                 | -    | -       | -10  | dB   |
| Output power of PA for 72.2 Mbps | 15.5 | 16.5    | 17.5 | dBm  |
| Output power of PA for 11b mode  | 19.5 | 20.5    | 21.5 | dBm  |
| DSSS, 1 Mbps                     | -    | -98     | -    | dBm  |
| CCK, 11 Mbps                     | -    | -91     | -    | dBm  |
| OFDM, 6 Mbps                     | -    | -93     | -    | dBm  |
| OFDM, 54 Mbps                    | -    | -75     | -    | dBm  |
| HT20, MCS0                       | -    | -93     | -    | dBm  |
| HT20, MCS7                       | -    | -73     | -    | dBm  |
| HT40, MCS0                       | -    | -90     | -    | dBm  |
| HT40, MCS7                       | -    | -70     | -    | dBm  |
| MCS32                            | -    | -89     | -    | dBm  |
| OFDM, 6 Mbps                     | -    | 37      | -    | dB   |
| OFDM, 54 Mbps                    | -    | 21      | -    | dB   |
| HT20, MCS0                       | -    | 37      | -    | dB   |
| HT20, MCS7                       | -    | 20      | -    | dB   |

## 6. Package Information

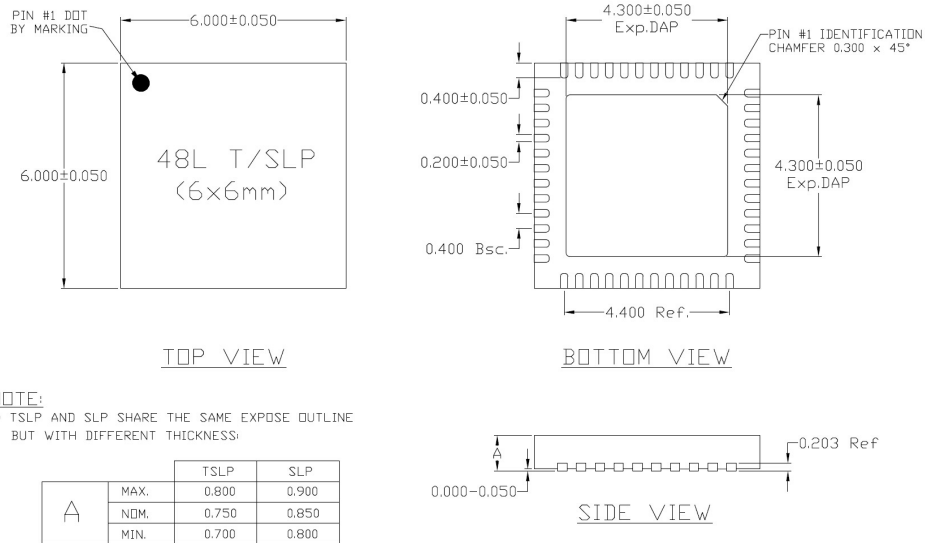


Figure 3: QFN48 Package

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## 7. Supported Resources

### 7.1 Related Documentation

The following links provide related documents of ESP32.

- [ESP32 Getting Started Guide](#)  
How to download ESP32-LAUNCHER firmware and configure with related tools.
- [ESP32 Programming Guide](#)  
How to program with ESP32 SDK, with some related programming examples.
- [ESP32 API Reference](#)  
Detailed description of ESP32 Application Programming Interfaces (APIs).

### 7.2 Community Resources

The following links connect to ESP32 community resources.

- [ESP32 Online Community](#)  
An Engineer-to-Engineer (E2E) Community for ESP32 at [www.esp32.com](http://www.esp32.com), where you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.
- [ESP32 Github](#)  
ESP32 development projects are freely distributed under Espressif's MIT license on Github. Established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding these devices.

## 8. Appendix - Touch Sensor

A touch sensor system is built on a substrate which carries electrodes and relevant connections with a flat protective surface. When a user touches the surface, the capacitance variation is triggered, and a binary signal is generated to indicate whether the touch is valid.

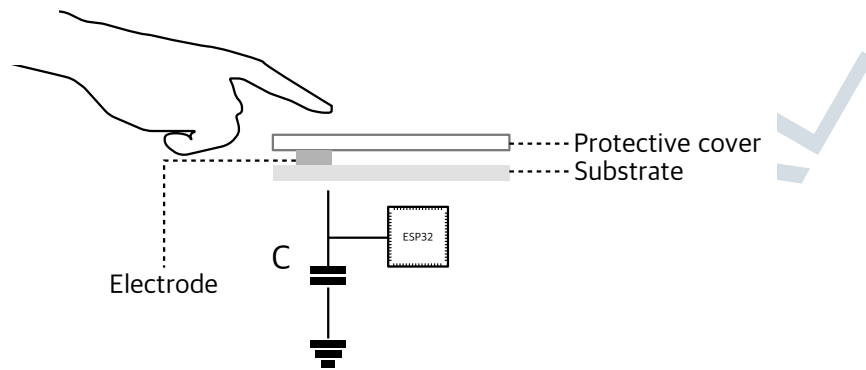


Figure 4: A Typical Touch Sensor Application

In order to prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

### 8.1 Electrode Pattern

The proper size and shape of an electrode helps improve system sensitivity. Round, oval, or shapes similar to a human fingertip is commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

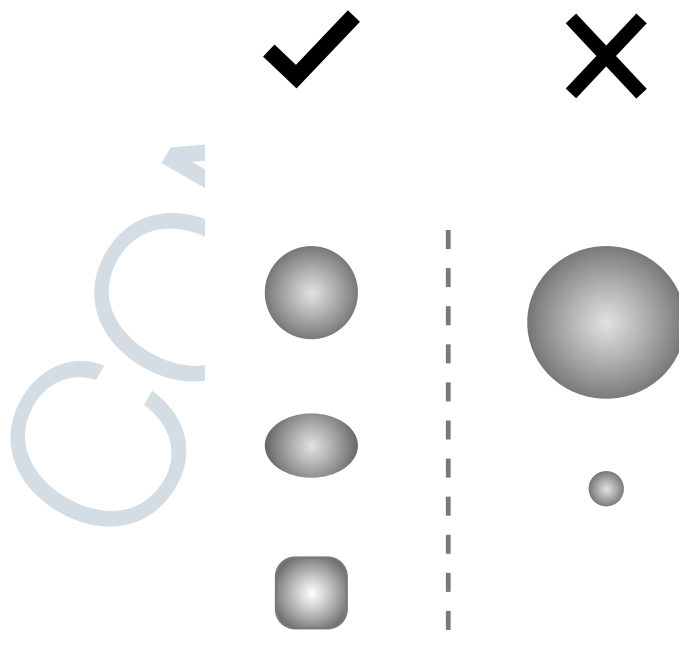


Figure 5: Electrode Pattern Requirements

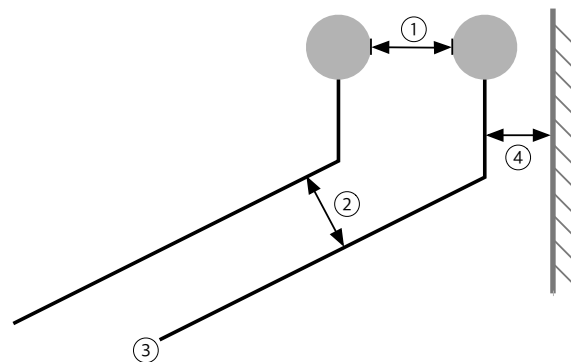
**Note:**

The examples illustrated in Figure 5 are not of actual scale. It is suggested that users take a human fingertip as reference.

## 8.2 PCB Layout

The recommendations for correctly routing sensing tracks of electrodes are as follows:

- Close proximity between electrodes may lead to crosstalk between electrodes and false touch detections. The distance between electrodes should be at least twice the thickness of the panel used.
- The width of a sensor track creates parasitic capacitance and may variations associated with manufacturing processes. The thinner the track is, the less capacitive coupling it generates. The track width should be kept as thin as possible and the length should not exceed 10cm to accommodate.
- We should avoid coupling with lines driving high frequency signals; the sensing tracks be routed parallel to each other on the same layer and the distance between the tracks should be at least twice the width of the track.
- When designing a touch sensor device, there should be no components adjacent to or underneath the electrodes.
- Do not ground the touch sensor device. It is preferable that no ground layer be routed under the device, unless there is a need to isolate it. Parasitic capacitance generated between the touch sensor device and the ground degrades sensitivity.



- ① Distance between electrodes - Twice the thickness of the panel
- ② Distance between tracks - Twice the track width
- ③ Width of the track (electrode wiring) - As thin as possible
- ④ Distance between track and ground plane - 2mm at a minimum

Figure 6: Sensor Track Routing Requirements